REMARKS/ARGUMENTS

Claims 1-39 were pending in the present application. By virtue of this response, no claims have been cancelled, claims 21 and 25 have been amended, and no new claims have been added. Accordingly, claims 1-39 are currently under consideration. Amendment and cancellation of certain claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented. No new matter has been added.

Concerning the Drawings

The Office Action required the Applicant to submit new corrected drawings in compliance with 37 CFR 1.121(d). With the Response, Applicant has submitted such new corrected drawings.

Rejections under 35 USC §102

Claims 1-3, 20-23 and 25 are rejected as allegedly being anticipated by Miller (U.S. Pat. 6,438,570).

Claim 1 of the present application recites, in part, a programmable logic device that includes at least one RAM block generating at least a first multi-bit calculation result. A shift operation is driven by a second multi-bit calculation result and a multi-bit adder adds the shifted second multi-bit calculation result to the first multi-bit calculation result.

In rejecting claim 1, the Office Action refers to Figure 4 of Miller which discloses a third order IIR filter 400. (Miller, col. 9, line 60). Filter 400 includes RAM 418 connected to a multiplier 430 that is connected to an adder 436. A second multiplier 432 is also connected to adder 436. (Miller, col. 10, lines 10-41; Fig. 4). Nowhere, however, does Miller disclose that RAM 418, or any other RAM shown in Figure 4, generates a first multi-bit calculation result, or a calculation result of any kind. Rather, Miller explains that an "input sample" is stored in RAM 416 and "gradually written to RAM 418". In short, no RAM of Figure 4 is disclosed to generate any calculation result.

Additionally, nowhere does Miller disclose a shift operation driven by a second multi-bit calculation result and that shifts the second multi-bit calculation result by at least one bit, as required by claim 1. Figure 4 of Miller discloses RAM 420 driving multiplier 432, which may generate a calculation result. But multiplier 432 directly drives adder 436, there is no shift operation between multiplier 432 and adder 436. And, multiplier 432 itself cannot be considered the shift operation recited in claim 1 because, for the same reasons discussed above with respect to multiplier 430, it does not operate on a multi-bit calculation result. Accordingly, nowhere is there disclosed a shift operation that shifts a second multi-bit calculation result.

Further, given that Miller does not disclose a shift operation that shifts a second multi-bit calculation result, Miller cannot disclose a multi-bit adder which adds a shifted second multi-bit calculation result to a first multi-bit calculation result, as required by claim 1.

Because Miller does not disclose a RAM block generating at least a first multi-bit calculation result, a shift operation that shifts a second multi-bit calculation result or a multi-bit adder that adds a shifted second multi-bit calculation result to a first multi-bit calculation result, claim 1 cannot be anticipated by Miller, and Applicant respectfully requests withdrawal of this rejection.

Claims 2, 3 and 20 are each dependent on claim 1. Because claim 1 cannot be anticipated by Miller, neither can be claims 2, 3 or 20, and applicant respectfully request withdrawal of these rejections.

With this response, independent claim 21 has been amended to add word "result" after the work multiplication in the third element of the claim. Amended claim 21 recites at least RAM block for generating at least a first multi-bit multiplication result, a shift operation driven by a second multi-bit multiplication result and that shifts the second multi-bit multiplication result by at least one bit and an adder adding the first multi-bit multiplication result to the second shifted multi-bit multiplication result. As discussed above with respect to claim 1, Miller does not disclose any of

these elements. Thus, Miller cannot anticipate claim 21 and Applicant respectfully requests withdrawal of this rejection.

Claims 22 and 23 are each dependent on claim 21. Because claim 21 cannot be anticipated by Miller, neither can be claims 22 or 23, and applicant respectfully request withdrawal of these rejections.

With this response, claim 25 has been amended to remove the word "the" from the first line. Amended claim 25 recites at least generating at least a first multi-bit calculation result from at least one LUT in at least one RAM block, shifting a second multi-bit calculation result to by at least one bit and adding the shifted second multi-bit calculation result to the first multi-bit calculation result. As discussed above with respect to claim 1, Miller does not disclose any of these elements. Thus, Miller cannot anticipate claim 25, and Applicant respectfully requests withdrawal of the rejection.

Claims 4-19, 24 and 26-39 are objected to as allegedly being dependent upon a rejected base claim. As discussed above, the base claims on which claims 4-19, 24 and 26-39 are believed to be allowable, thus claims 4-19, 24 and 26-39 are also believed to be allowable and Applicant respectfully requests withdrawal of the objection.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 306812004220. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: April 11, 2005

Respectfully submitted,

By_____

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Attachments

In the drawings

The attached sheet(s) of drawings include Figures 1-14, replacing the original sheets including Figures 1-14.

Attachment: Replacement sheets 1-8.